Switched Quasi Impedance-Source DC-DC Network for Photovoltaic Systems

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Abstract- The development of renewable energy power systems which are primarily based on solar energy is accelerating as a consequence of the global diminution of fossil fuels. The solar energy is a vast, clean and an inexhaustible resource which can be harnessed by using the photovoltaic (PV) technology. In order to obtain greater voltages from the PV power system for the grid-connected inverters, a DC-DC boost converter might be employed. However, due to the various limitations of the traditional boost converters, many configurations have been proposed to enhance their boost ability. The Quasi impedance-source DC-DC network is one such topology which has been derived from the conventional Z-source DC-DC network by equipping its output ports with a switch and a diode. When compared with the existing Z-source based configurations, it has a lower duty cycle (less than 0.25) which produces a higher boost factor, it has a high voltage gain and it can also avert the instability which is caused due to the saturation of the inductors. It has been developed with a fewer number of energy elements which leads to reduced losses, reduction in cost and enhanced power density. The features of the proposed network along with its working principle in continuous conduction mode for steady state condition, components' voltage and current stresses are assessed. The MATLAB/Simulink findings are offered to back up the theoretical analysis. and attributes listed above.

Keywords Photovoltaics, Quasi Z-source, Grid-connected inverter, Z-source DC-DC converter.

Nomenclature

C_X	Capacitor X
C_Y	Capacitor Y
Cz	Capacitor Z
D_X	Diode x
D_Y	Diode y
D_Z	Diode z
F_S	Switching frequency
I_{DX}	Current of diode x

I_{DY}	Current of diode y
I_{DZ}	Current of diode z
I_{in}	Input current of the converter
I_{LX}	Current of inductor L_X
I_{LY}	Current of inductor y
I_0	Output current
I_{SX}	Current of switch x
I_{SY}	Current of switch y
L_X	Inductor x
P_0	Output power
R	Load Resistance
S_X	Switch x
S_Y	Switch y
V_{CX}	Voltage of capacitor C_X
V_{CY}	Voltage of capacitor C_Y
V_{CZ}	Voltage of capacitor C_Z
V_i	Input voltage of the converter
V_{LX}	Voltage of inductor L_X
V_{LY}	Voltage of inductor L_Y
V_0	Output voltage of the converter
ΔI_L	Ripple current of inductors
ΔV_C	Ripple voltage of capacitors

1. Introduction

The global energy crisis has prompted to look for alternative energy sources [1-3]. One such evolving technology is the Photovoltaic technology which harnesses the solar energy and converts it into electrical energy. Solar energy is clean, abundant in nature, and it helps to mitigate climate change, making PV power generation a front runner to solve the energy crisis. The photovoltaic cells are made up of PN junction diodes. Depending on the semiconductor and the built-up method, a photovoltaic cell yields a voltage between 0.5 and 0.8 volts. A PV module is formed by connecting multiple PV cells in series to get a larger output voltage. To create a PV panel, these modules might be joined either in series or in parallel. The PV system is highly advantageous as it can be installed easily and requires minimal maintenance. As it has no moving parts, it is sturdy and noiseless. One of the major drawbacks is that the PV arrays are a low- voltage direct current source whose voltage varies widely with temperature and irradiation.

Hence, they require a high step-up stage like a boost converter to give a higher output to the grid-connected inverter for PV applications as illustrated in Figure 1. Despite having a simple and economical design the traditional boost converter is not suitable when the component voltage stress is large and for high power applications. The boosting mode has limitations because of parasitic resistances and component voltage dips. High voltage gain may only be achieved by using complex structures, which have more components, thereby decreasing the efficiency and increasing the cost.

In [4], a Z-source converter is proposed which consists of a novel X-shaped impedance network that connects the converter primary circuit towards the power supply as illustrated in Figure 2. The problem of restricted output voltage in the traditional boost converter can be resolved. The Z-source network was first presented in 2002 by Peng with 1/(1-2D) as its boost factor. The intended impedance-source converter is flexible and can be utilized to convert power from dc to dc, ac to ac, ac to dc and dc to ac. Until now, more emphasis has been on dc-ac power conversion but recently many topologies which are attained from the Z-source for dc-to-dc conversion have also been designed and it is becoming a rapidly expanding area of research. The Z-source converter has discontinuous input side current, high voltage stress over capacitors and no familiar ground; therefore, its applications are limited.

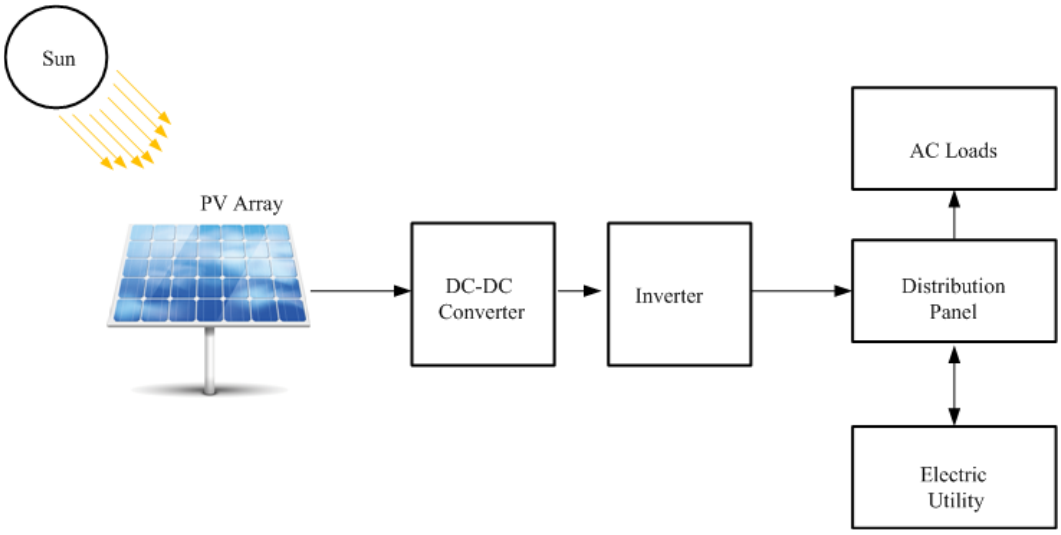


Fig. 1 The grid-connected PV system.

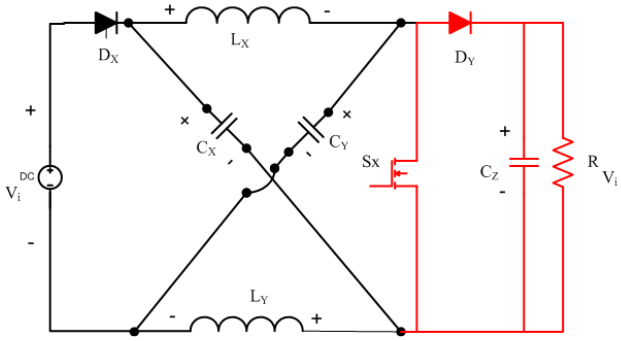


Fig. 2. Circuit topology of the conventional converter

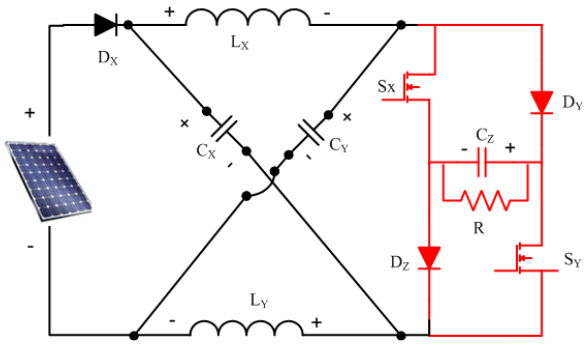


Fig. 3 Circuit topology of proposed of SQZS converter

To counteract the drawbacks of the conventional Impedance-source network, a quasi Z-source network with the same boost factor was proposed [5,6]. Many methods such as switched-component techniques [7,8], voltage multiplier technique [9], voltage lift technique [10], have been presented to increase the boost factor. A hybrid Impedance-source dc-dc converter is proposed in [11] to escalate the voltage gain further. The hybrid Impedance-source dc-dc converter achieves the greater voltage gain of 1/(1-4D). However, the use of several energy elements will result in low efficiency and high cost. Here, a Switched Quasi Impedance-source DC-DC converter (SQZSC) is intended which has a simplified circuitry to attain a higher voltage gain. It is accomplished by modifying the conventional Impedance-source converter's rear end to include a diode and a switch. When the switches are turned on, the load side capacitor serves as filter capacitor and is also linked in sequence in accordance with the energy storing loops of the inductors.

The boost factor is raised to 1/(1-4D), it is identical to the boost factor of the complex hybrid impedance-source dc to dc converter but the number of energy components is drastically decreased thereby, enhancing the converter efficiency and lowering the cost. In comparison to the previous Impedance-source based converters, a larger voltage gain is achieved with a lower duty factor (less than 0.25) to prevent the irregularity brought on by the saturated inductors.

The work consists of 6 sections and is constructed as follows. The working principle and analysis of the Proposed Converter is conferred in Section 2. Section 3 analyses the voltage and current parameters of proposed converter's components. The intended converter is contrasted with current converter topologies in Section 4. The simulation results and relevant discussions are illustrated in Section 5. Finally, the conclusion and future scope are discussed in Section 6.

2. Operating Principles and Analysis of the Proposed Converter

2.1 Configuration of the Proposed Converter

Figure 3 illustrates the proposed Switched Quasi Impedance-source Converter (SQZSC) topology. It is obtained by the addition of two components namely a diode (D_Z) and a switch (S_Y) at the tail side of the traditional Z-

source topology. The capacitor (C_Z) has two convenient functions, which is to perform as a filter capacitor and to deliver the energy to inductors by discharging when both the switches (S_X and S_Y) are switched on simultaneously. The boost factor of the modified topology is notably enhanced at a level of 1/(1-4D). In comparison to hybrid Impedance-source dc-dc converter [11], the proposed topology attains the same load side voltage with less number of energy elements which in turn leads to reduced cost, reduction in size and bulkiness of the converter with improved power density. Moreover, this topology deals with reduced voltage stresses on capacitors when compared with the switched Z-source networks. The circuit operates in continuous conduction mode. By the various combinations of the duty cycles, load resistor and inductances the operation of the Switched Quasi Z-source converter is partite into two states (State-A and State-B). For directness, a few presumptions are made, namely: 1.the circuit elements are in ideal condition 2. $L_X = L_Y$ and $C_X = C_Y$ 3. the diodes which are in anti-parallel with the switches are ignored.

State-A

Figure 4, figure 5 & figure 6 illustrates the State-A operating loops of SQZSC. In this state, both the switches S_X and S_Y are switched on concurrently and the diodes D_X, D_Z and D_Y are reverse biased, hence $i_{DX} = i_{DY} = i_{DZ} = 0$. The inductors L_X and L_Y store energy as the capacitors C_X and C_Y get discharged, while capacitor C_Z feeds the load. From the Figure 3, the current passing through the capacitor C_X is same as the current flowing in the inductor L_X i.e., $i_{CX} = i_{LX}$; similarly, the capacitor C_Y has the same current with the inductor L_Y, $i_{CY} = i_{LY}$. The currents in the switches are also same, i.e., $i_{SX} = i_{SY}$. From Figure 4, on applying KCL,

$$i_{SX} = i_{LX} + i_{LY} \quad (1)$$

$$i_{CZ} = i_{SX} + i_O \quad (2)$$

From Figure 5 and figure 6, on applying KVL,

$$v_{Lx} = v_{Cx} + v_{Cz} \quad (3)$$

$$v_{Ly} = v_{Cy} + v_{Cz} \quad (4)$$

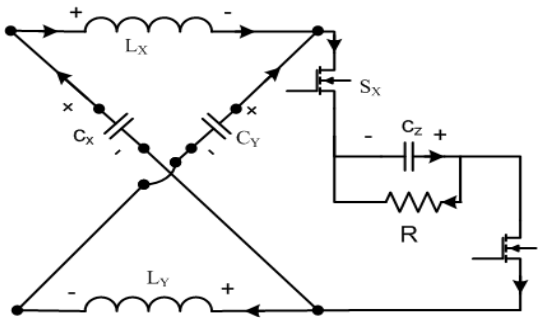
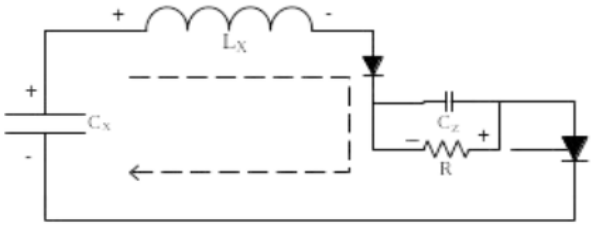


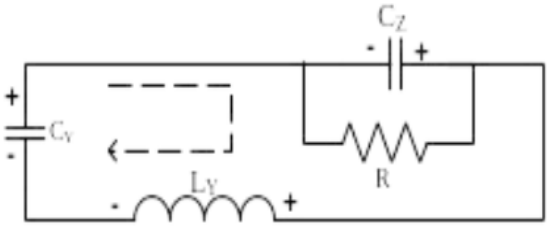
Fig. 4. KCL loops of the proposed SQZSC in State A.



$$+V_{Lx} - V_{Cz} - V_{Cx} = 0$$

$$V_{Lx} = V_{Cz} + V_{Cx}$$

Fig. 5. KVL loops of the proposed SQZSC in State-A.



$$-V_{CY} - V_{CZ} + V_{LY} = 0$$

$$V_{LY} = V_{CY} + V_{CZ}$$

Fig. 6. KVL loops of the proposed SQZSC in State-A.

State - B

Figure 7 and Figure 8 represent the State-B working loops of the proposed SQZSC. In this state, the diode D_X, D_Y and D_Z are forward biased and both the switches S_X and S_Y are turned off i.e., $i_{SX} = i_{SY} = 0$. The source voltage V_i, inductor L_Y and inductor L_X discharge their energies to capacitors C_X and C_Y respectively. Similarly, the energy is transmitted to capacitor C_Z and load resistor by the source voltage V_i and by both the inductors L_X and L_Y. It can be noted from Figure 8 that the current passing through the diodes D_X and D_Y are same.

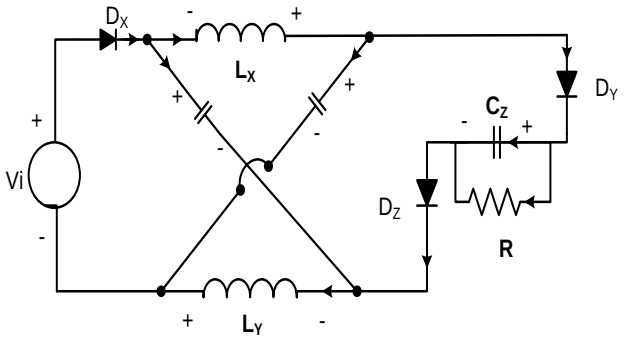


Fig. 7. KCL loops of the proposed SQZSC in State-B.

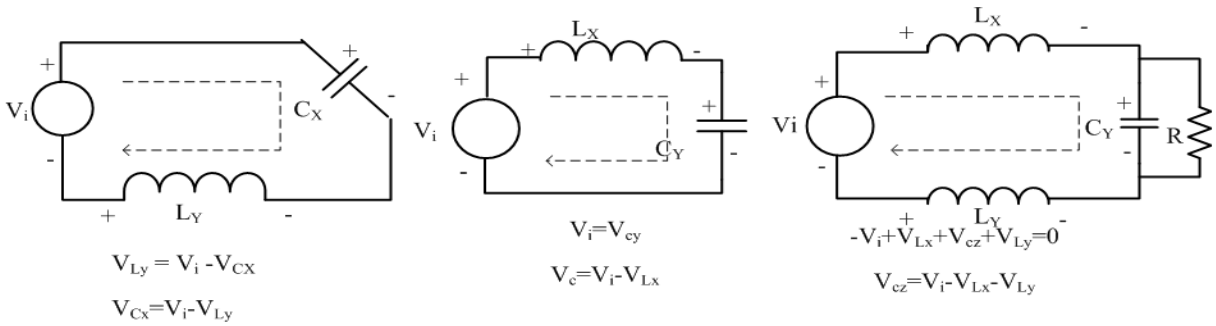


Fig. 8. KVL loops of the proposed SQZSC in State-B

From Figure 7, on applying KCL,

$$i_{DX} = i_{LX} - i_{CX} \quad (5)$$

$$i_{DY} = i_{LX} + i_{CY} \quad (6)$$

$$i_{DZ} = i_O - i_{CZ} \quad (7)$$

From Figure 8, on applying KVL, the voltages over the three capacitors in this state can be obtained as:

$$V_{CX} = V_i - V_{LY} \quad (8)$$

$$V_{CY} = V_i - V_{LX} \quad (9)$$

$$V_{CZ} = V_i - V_{LX} - V_{LY} \quad (10)$$

The Z-source network's symmetry facilitates in acquiring the following equations for both the states.

$$i_{LX} = i_{LY} \quad (11)$$

$$V_{LX} = V_{LY} \quad (12)$$

$$i_{CX} = i_{CY} \quad (13)$$

$$V_{CX} = V_{CY} \quad (14)$$

3. Parameters of the Proposed SQZSC

Given that the source and output side voltages are linearly related to the duty cycle of switches SX and SY. The boost factor of the proposed SQZSC, the element voltages and currents in CCM are deduced according to the analyses of given two states.

3.1. Boost factor and component voltage stresses

By volt-sec balance principle,

$$V_{on}T_{on} + V_{off}\,T_{off} = 0 \quad (15)$$

The duty ratio is given as a ratio of on time period to the total time period, therefore,

$$T_{on} = DT;\ T_{off} = (1 - D) \quad (16)$$

For inductor L_X;

During energy storage, $V_{LX} = V_{CX} + V_{CZ}$
During energy release, $V_{LX} = V_{CX} - V_{CZ}$

By using Voltage-second balance principle for inductor L_X;

$$V_{LX}T_{on} + V_{LX}T_{off} = 0 \quad (17)$$

Substituting (16) in (17) results in

$$V_{LX}D + V_{LX}(1 - D) = 0 \quad (18)$$

By expanding (18) we get,

$(V_{CX} + V_{CZ})D + (V_{CX} - V_{CZ})(1 - D) = 0$
$V_{CX}D + V_{CZ}D + V_{CX} - V_{CX}D - V_{CZ} + V_{CZ} = 0$
$V_{CZ}(2D - 1) + V_{CX} = 0$

The final equation for boost factor of capacitor C_Z with respect to C_X is given as:

$$V_{CZ} = V_{CX}(1 - 2D) \quad (19)$$

Similarly for inductor L_Y;
During energy storage, $V_{LY} = V_{CY} + V_{CZ}$
During energy release, $V_{LY} = V_i - V_{CX}$

By using Voltage-second balance principle for inductor L_X;

$$V_{LY}T_{on} + V_{LY}T_{off} = 0 \quad (20)$$

Substituting (16) in (20),

$$V_{LY}D + V_{LY}(1 - D) = 0 \quad (21)$$

By expanding (22) we get,

$$(V_{CY} + V_{CZ})D + (V_i - V_{CX})(1 - D) = 0$$
$$V_{CY}D = V_{CZ}D + V_i - V_iD - V_{CX} + V_{CX}D = 0 \quad (\text{since } V_{CX} = V_{CY})$$

$$V_{CX}D + V_{CZ}D + V_i - V_iD - V_{CX} + V_{CX}D = 0$$
$$V_{CX} = ((2D2 - 3D + 1)/(4D2 - 5D + 1))V_i \quad (22)$$

Substituting (19) in (22) we get,

$$V_{CX} = (2D2 - 3D + 1/4D2 - 5D + 1)V_i$$
$$V_{CX} = V_{CY} = ((1 - 2D)/(1 - 4D))V_i \quad (23)$$

Substituting (19) in (22) we get,

$$V_{CX}D + V_{CZ}D + V_i - V_iD - V_{CX} + V_{CX}D = 0$$

By taking V_{CX} and V_i common, the above equation can be deduced as,

$$V_{CX}(2D\text{-}1) + V_{CZ}D + V_i(1 - D) = 0$$

Substituting V_{CX} value in below equation we get,

$$V_{CZ}(2D\text{-}1\text{-}4D2 + 2D + D) + V_i(1\text{-}D) = 0$$
$$V_0 = V_{CZ} = 1/(1 - 4D)V_i \quad (24)$$

Hence, the capacitor voltages and output voltage are given as:

$$V_{CX} = V_{CY} = (1 - 2D)/(1 - 4D)V_i \quad (25)$$

$$V_0 = V_{CZ} = (1/(1 - 4D))V_i \quad (26)$$

where D is denoted as duty cycle of switches S_X and S_Y. The suggested converter has the voltage gain of 1/(1-4D), it is similar to the hybrid Impedance-source dc-dc converter in [11]. The diodes D_X, D_Y, and D_Z can sustain reverse voltages of $2V_i/(1-4D)$, $V_i/(1-4D)$ and $V_i/(1\text{-}4D)$ subsequently, when the switches S_X and S_Y are switched on at the same time. When the switches are off, they have the similar blocking voltage, which is equal to $V_i/(1\text{-}4D)$.

3.2. Current stresses of Inductors, Diodes and Switches

Given that under ideal circumstances, input side and output side powers are identical, the input current I_i may be represented as output side current I_0 as follows:

$$V_i I_i = V_0 I_0$$
$$I_i = (V_0 I_0)/V_i$$
$$I_i = (V_i I_0)/(1 - 4D)$$

Since $V_0 = 1/(1 - 4D)V_i$

$$I_i = 1/(1 - 4D)I_0 \quad (27)$$

Since the input voltage source and diode D_X are linked in series, their currents, I_i and i_{DX}, are equal. Therefore, it is possible to get the average input current I_i as:

$$I_i = \frac{1}{T}\int_{DT}^{T} i_{Dx}dt \quad (28)$$

$$I_i = \frac{1}{T}\int_{0}^{T} i_{Lx}dt \quad (29)$$

$$I_i = I_{Lx} = I_{Ly} = \frac{1}{1 - 4D} I_o \quad (30)$$

Where I_{LX} and I_{LY} are the average currents through the inductors L_X and L_Y, respectively.

The component current stresses can be obtained as

$$I_{DX} = (1/(1 - 4D))I_0 \quad (31)$$

$$I_{DY} = I_{DZ} = (1 - 2D)/(1 - 4D)I_0 \quad (32)$$

$$I_{SX} = I_{SY} = (2D/(1 - 4D))I_0 \quad (33)$$

Where I_{DX}, I_{DY}, I_{DZ}, I_{SX} and I_{SY} are the average currents through D_X, D_Y, D_Z, S_X and S_Y.

3.3. Determination of Inductance and Capacitance

INDUCTANCE: The inductance values in the proposed converter, $L_X = L_Y$. The inductance can be calculated by considering that the inductor has a peak-to-peak current ripple of Δi_L

$$L_X = L_Y = \frac{2V_i D(1 - D)}{\Delta i_L I_o f_s} \quad (34)$$

For D=0.19, V_i = 12V, f_s =20 kHz and i_L=0.5, the values of L_X & L_Y are given 184.68 μH.

$$C_X = C_Y = \frac{I_o D}{\Delta v_c f_s V_i (1-2D)} \quad (35)$$

For D = 0.19, I_0 = 2A, f_s = 20kHz, ΔV_C =0.5 and V_i= 12V. The value of C_X, C_Y are given by C_X = C_Y= 5.10 μF.

4. Comparison with Existing Topologies

Table 1 compares the converter's effectiveness as intended with the converters proposed in [10]-[16] in provision of energy elements and voltage gain. Figure 9 shows a visual representation of the voltage gain as a consequence of the converters' duty ratio. When compared with the previously intended converters for the same duty ratio, it may be inferred that the intended converter generates a largest boost factor. Table 1 shows that the typical boost converter's uses are restricted since it is unable to contribute a significant voltage gain. The proposed SQZSC generates a high boost factor, 1/(1-4D), which is identical to the Hybrid Z-Source Boost DC-DC Converter accorded in [17-22], but it has the benefit of using fewer number of energy elements which lowers the converter's cost, size, and bulk. The suggested converter offers a variety of applications because of its benefits.[23-29].

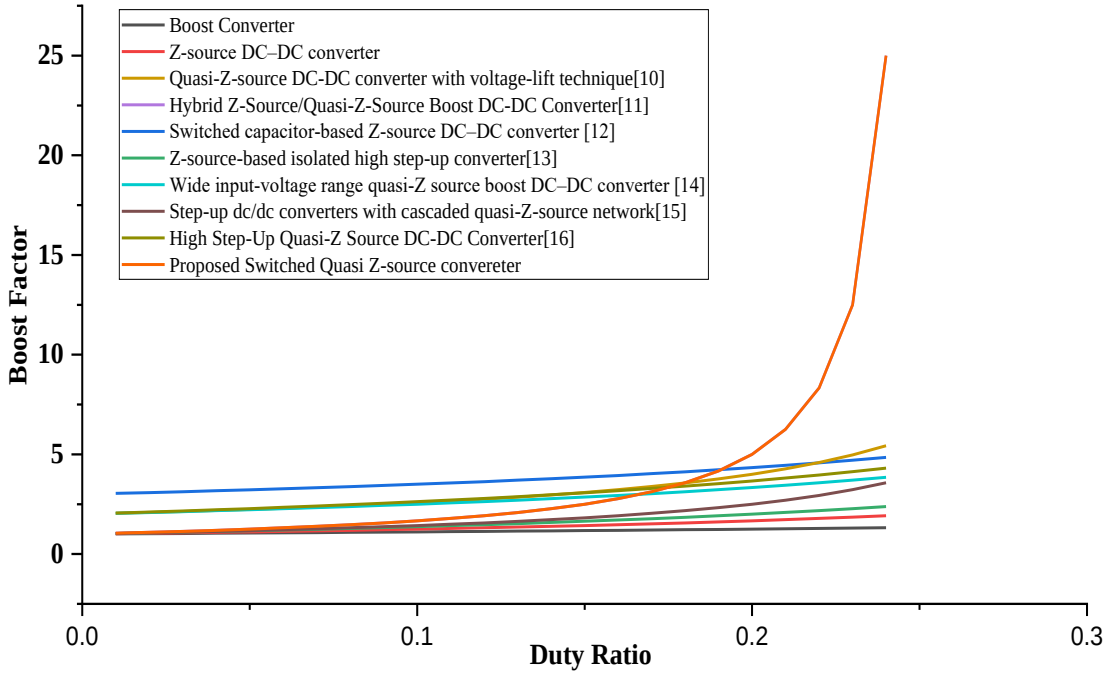


Fig. 9. Relationships between the voltage gain and the duty ratio.

Table 1. Comparison of the intended SQZSC with different converter topologies.

S No	Converter	No. of inductors	No. of capacitors	No. of diodes	No.of power switches	Total no. of components	Voltage gain	Maximum voltage stress across power switches and diodes
1	Boost converter	1	1	1	1	4	1/ (1 − D)	V_{in}/(1-D)
2	Z-source DC–DC converter	2	3	2	1	8	1/ (1 − 2D)	V_{in}/(1-2D)
3	Quasi-Z-source DC-DC converter with voltage-lift technique [10]	4	4	3	1	12	2(1 − D)/ (1 − 3D)	2 V_{in} (1 − D)/(1 − 3D)
4	Hybrid Z-Source/Quasi-Z-Source Boost DC-DC Converter [11]	4	7	4	1	15	1/(1-4D)	V_{in} /(1-4D)

5	Switched capacitor-based Z-source DC–DC converter [12]	2	5	4	1	12	$(3-2D)/(1-2D)$	$V_{in}/(1\text{-}2D)$
6	Z-source-based isolated high step-up converter [13]	3	5	4	1	13	$(n(1+D))/(1-2D)$	$V_{in}/1-2D$
7	Wide input-voltage range quasi-Z source boost DC–DC converter [14]	2	5	4	1	12	$2/(1-2D)$	$V_{in}/(1\text{-}2D)$
8	Step-up dc/dc converters with cascaded quasi-Z-source network [15]	3	5	3	1	12	$1/(1-3D)$	$V_{in}/(1\text{-}3D)$
9	High Step-Up Quasi-Z Source DC-DC Converter [16]	3	7	5	1	16	$(2+D)/(1-2D)$	$V_{in}/(1\text{-}2D)$
10	Proposed Switched Quasi Z-source Converter	2	3	3	2	10	$1/(1\text{-}4D)$	$V_{in}/(1\text{-}4D)$

5. Simulation Results

To determine the viability and potency of the proposed SQZS converter, simulation is carried out. As shown in the table 2 the input voltage is fed from photovoltaic cells with a magnitude of 12V (Average value of a solar module). The pre-assigned parameters are as follows: (1) The input voltage, Vin = 12 V; (2) the output power, P_O =100W; (3) the switching frequency, f_s= 20000 H; (4) the duty ratio, D= 0.19; (5) the inductor values, $L_X = L_Y$=184.68 μH; (6) the capacitor values, $C_X = C_Y$= 5.18 μF; (7) the filter capacitance, C_Z= 300 μF and (8) the load resistance, R=25. The related waveforms for the input side voltage and current, capacitor voltage and current, inductor current, switch and diode voltages and the output side voltage and current are depicted. Figure 10 represents the input dc voltage of 12V. The graphical representation of input current in accordance to time is shown in Figure 11, for proper demonstration a steady state segment with two complete cycles is exhibited. As the diodes are switched on and off, the input current varies between 0A and 19A. The capacitors C_X and C_Y discharge the energy when the active switches are switched on and charges when the switches are in off state.

The graphical representation of capacitor voltages in accordance to time is shown in Figure 12. Three cycles are taken on the x-axis for steady state representation. The x-axis ranges from 0.66 to 0.6601 seconds and voltage ranges from 15 to 30 V. The graphical representation of capacitor currents in accordance to time is shown in Figure 13. The simulated currents are altered between -10 to +10 A and the x-axis ranging from 0.66 to 0.6601 seconds. The inductors L_X and L_Y are charged when the active switches are in on state and they discharge their energy when the active switches are in off state which is depicted in Figure 14.

A segment of steady state portion is demonstrated with four complete cycles. The voltages across the diodes and switches are depicted in Figure 15 and Figure 16 respectively. The diodes and switches are operated with a duty ratio of 19% and they are turned on and off (altered for 20000 times in a second) i.e, switching frequency is 20000 Hz with a voltage magnitude of 98.6 V and 47.8 V respectively. For a 100W power, the intended converter is designed with an output voltage of 50V. Figure 17 represents the simulated DC output voltage. A load of 25Ω resistance is used at the output and hence the DC output current can be given as 2A theoretically. Figure 18 depicts the simulated output current waveform. The simulated value is approximately 1.901A and is much closer to the computed theoretical value.

Table. 2 Simulation Parameter

Component	Description	Specification
V_{in}	Input Voltage	12V
V_o	Output Voltage	50V
P_o	Output Power	100W
f_s	Switching frequency	20000 Hz
R_o	Load resistor (R)	25 Ω
$M(D) = V_o/V_i$	Gain	4.16
D	Duty ratio	0.19
L_x, L_y	Inductor	184.68 µH
C_x, C_y	Capacitors	5.10 µF
C_z	Filter Capacitor	300 µF

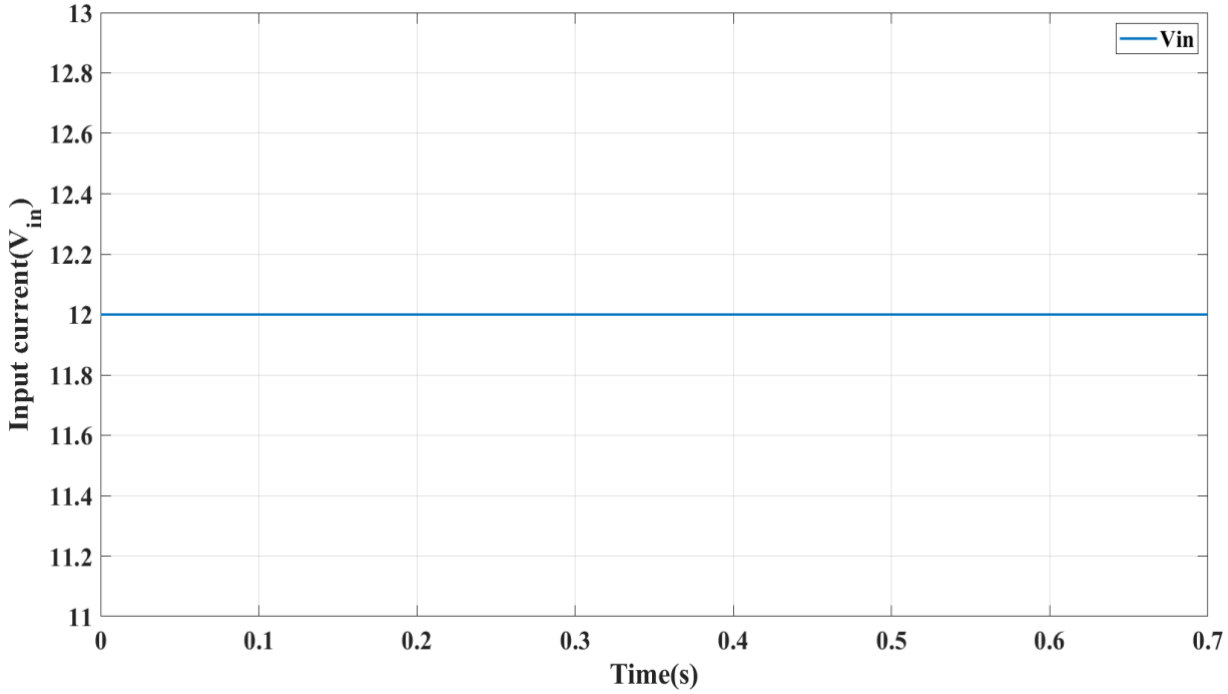


Fig. 10. Simulated waveform of the input voltage

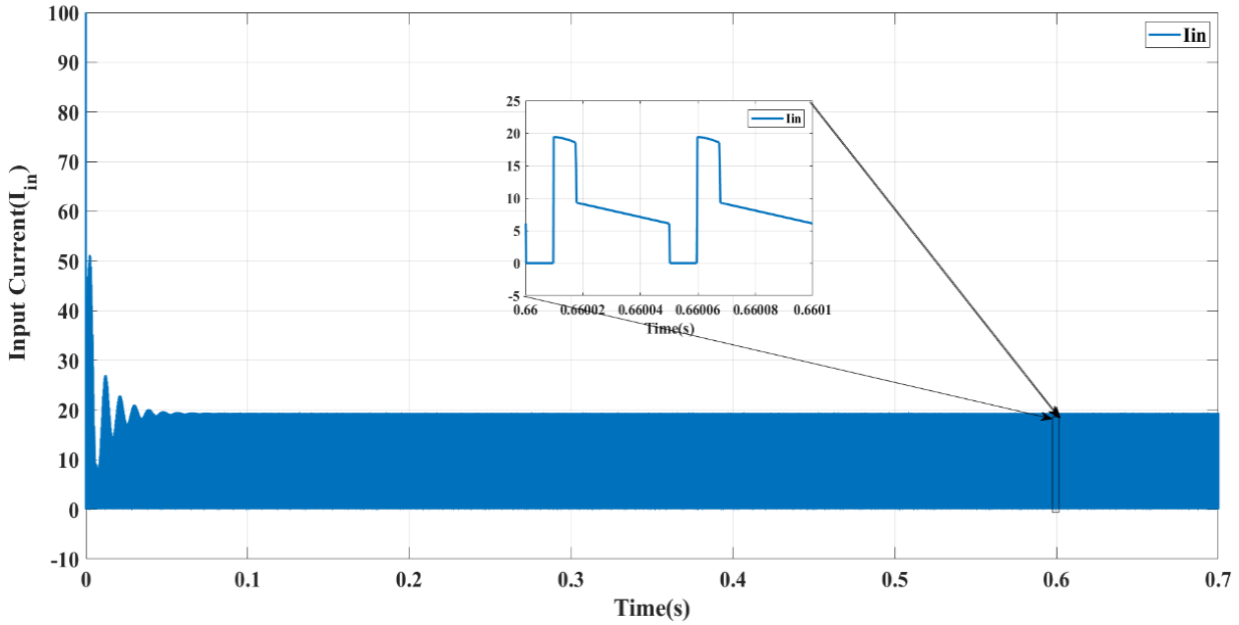


Fig. 11. Simulated waveform of the input current.

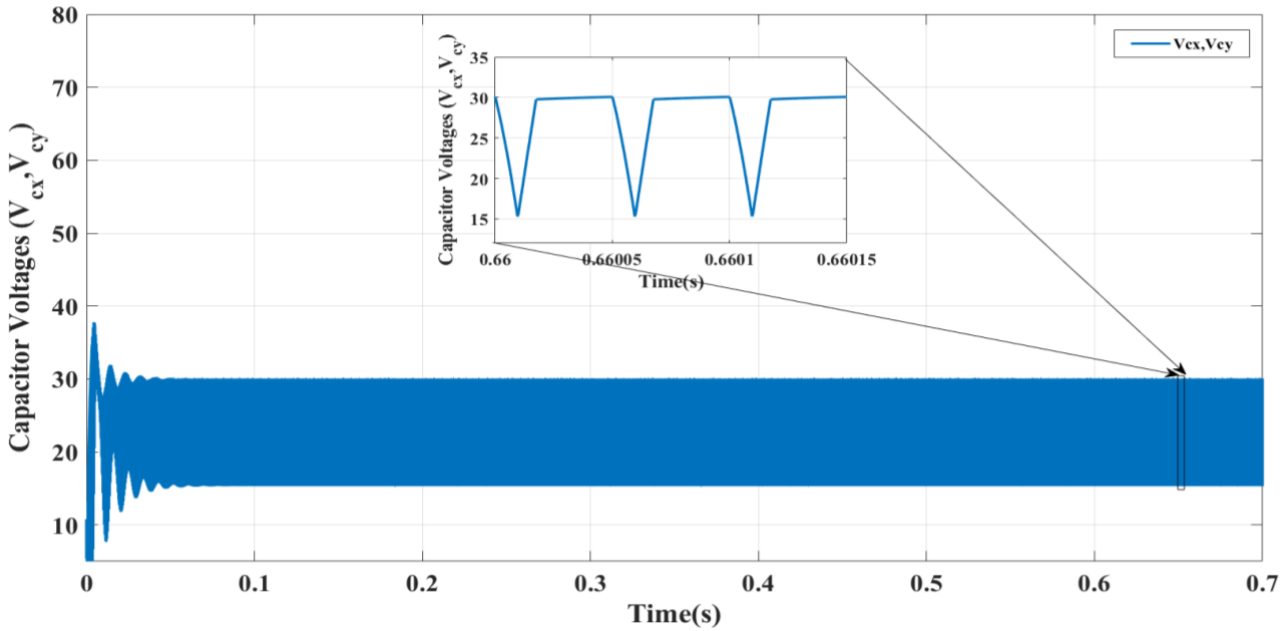


Fig. 12. Simulation waveforms of Capacitor voltages (V_{CX} and V_{CY}).

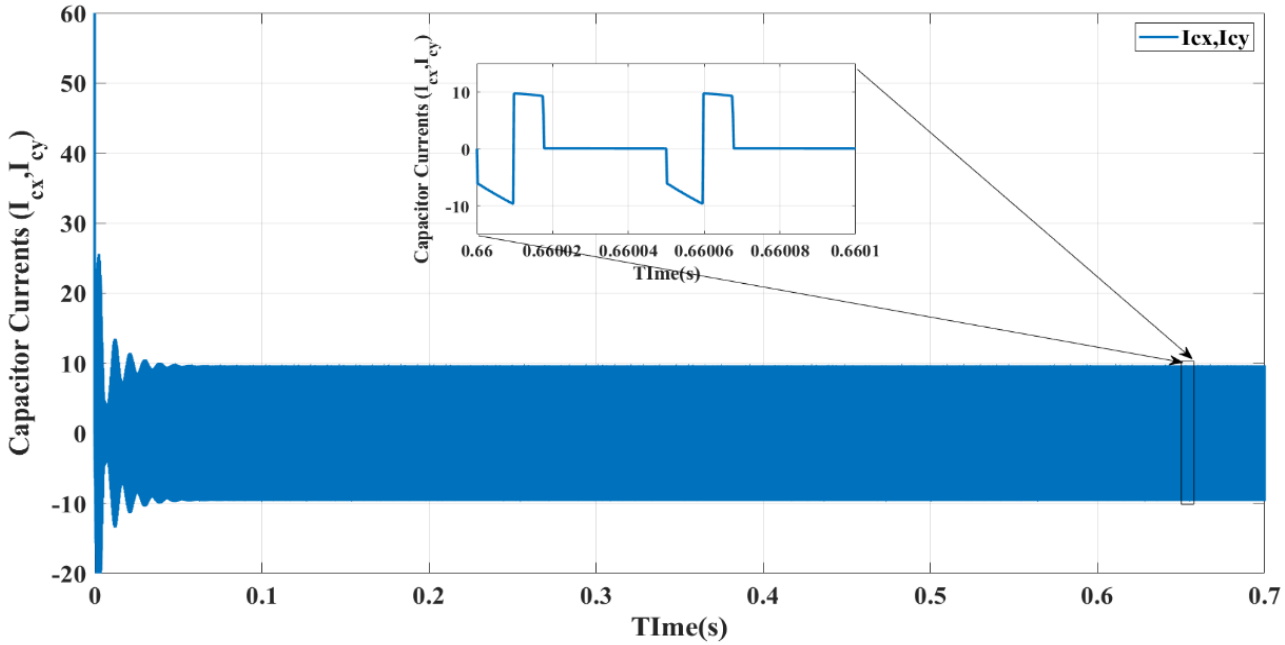


Fig. 13. Simulation waveform of Capacitor currents (I_{CX} and I_{CY}).

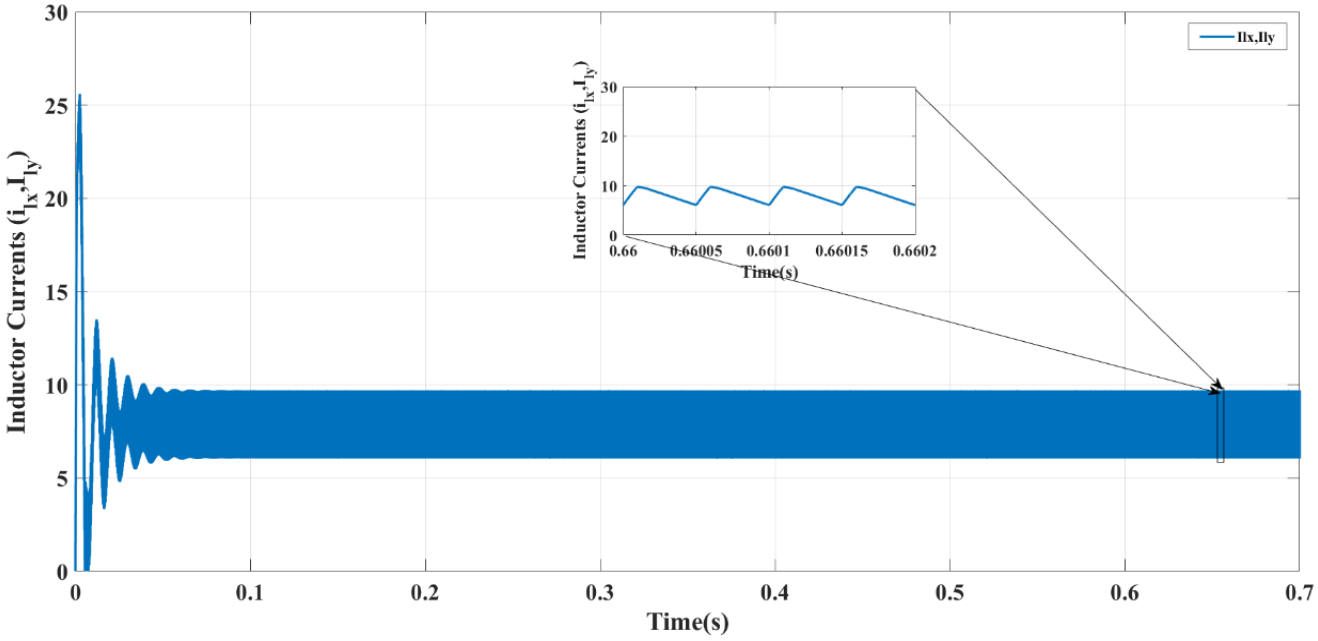


Fig. 14. Simulation waveform of Inductor currents (I_{LX} and I_{LY}).

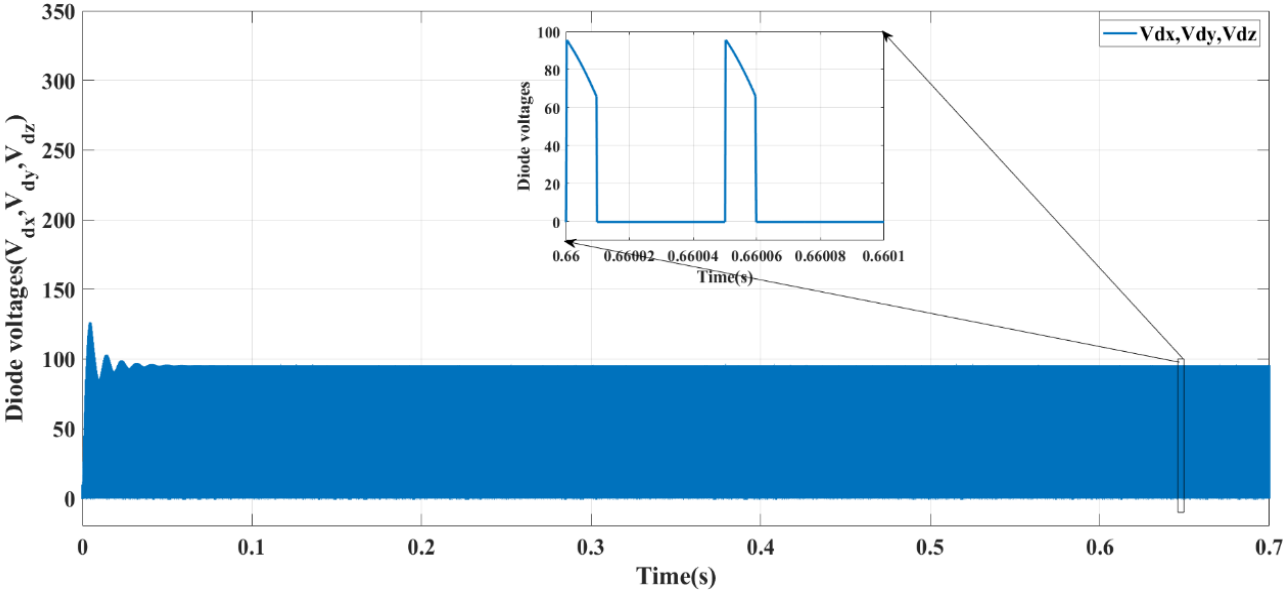


Fig. 15. Simulation waveform of Diode voltages (V_{DX}, V_{DY} &V_{DZ}).

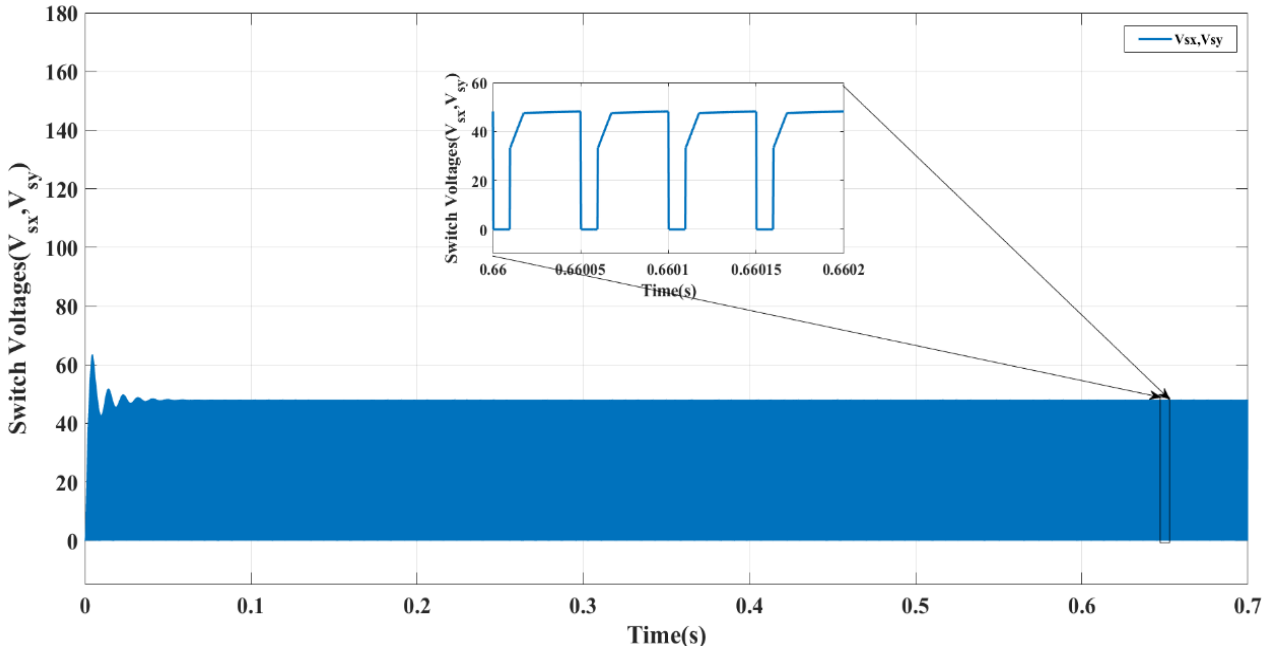


Fig.16. Simulation waveform of Switch Voltages (V_{SX} and V_{SY}).

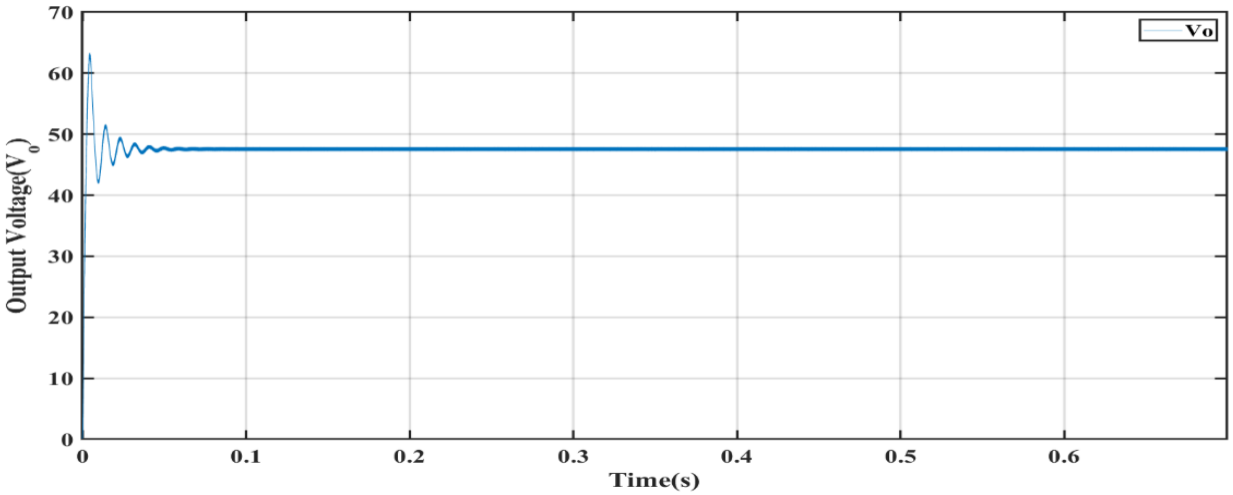


Fig.17.Simulation waveform of Output voltage waveform.

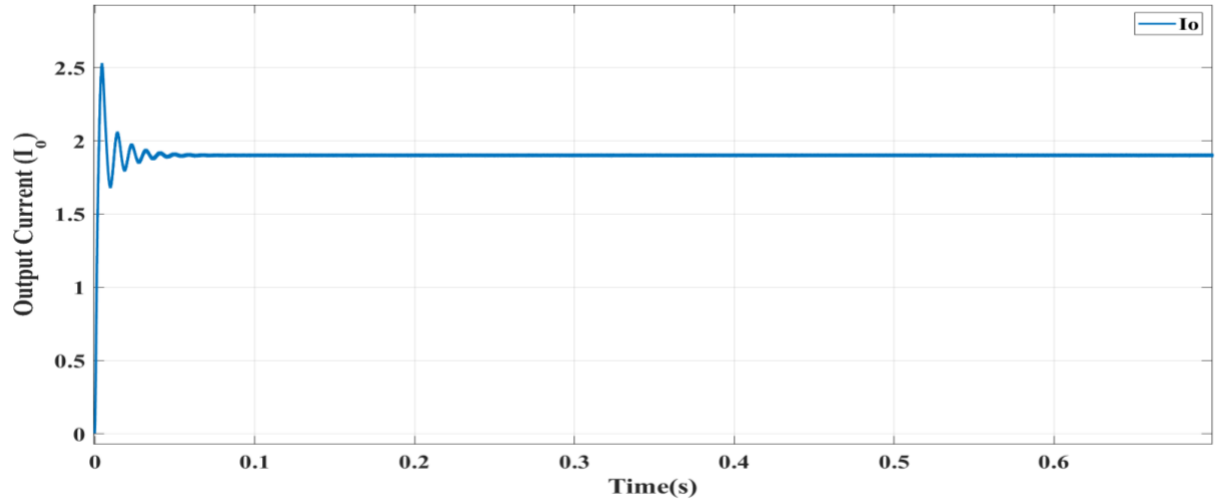


Fig. 18. Simulation waveform of Output current waveform.

Table 3. Simulated parameters for various duty ratios.

D	V_{in}	I_{in}	P_{in}	V_{SX},V_{SY}	V_0	I_0	P_0	Efficiency	Regulation
5	12	0.713	8.556	14.71	14.09	0.5635	7.94	92.797043	0.14194464
6	12	0.7748	9.2976	15.17	14.69	0.5876	8.63	92.8394855	0.19060585
7	12	0.8836	10.6032	16.23	15.7	0.6279	9.86	92.9722159	0.22292994
8	12	0.9692	11.6304	16.96	16.45	0.6578	10.8	93.0393184	0.23100304
9	12	1.122	13.464	18.39	17.71	0.7084	12.5	93.1800654	0.29926595
10	12	1.245	14.94	19.17	18.66	0.7465	13.9	93.2375502	0.33226152
11	12	1.471	17.652	20.89	20.29	0.8118	16.5	93.3119307	0.37949729

12	12	1.657	19.884	21.75	21.55	0.8619	18.6	93.4115118	0.44083527
13	12	2.009	24.108	24.04	23.74	0.9494	22.5	93.4907748	0.51811589
14	12	2.308	27.696	25.83	25.45	1.018	25.9	93.5445552	0.58546169
15	12	2.899	34.788	28.90	28.54	1.142	32.6	93.6894331	0.68675543
16	12	3.427	41.124	28.98	31.04	1.242	38.6	93.7449664	0.77319588
17	12	4.531	54.372	36.05	35.71	1.428	51	93.7870227	0.94371325
18	12	5.587	67.044	40	39.69	1.587	63	93.9502864	1.06072058
19	12	8.019	96.228	47.8	47.52	1.901	90.3	93.8765432	1.29840067
20	12	10.63	127.56	54.82	54.7	2.188	120	93.8225149	1.59597806
21	12	17.71	212.52	71	70.58	2.823	199	93.7546302	1.88863701
22	12	27.2	326.4	88.42	87.32	3.493	305	93.4463113	2.5526798
23	12	57.1	685.2	126.5	125.9	5.037	634	92.5508319	73.6624305
24	12	60.7	728.4	130.4	129.7	5.19	673	92.4139209	3.84656901

The performance of the intended SQZS converter in provision of efficiency, regulation, output power, output voltage, stresses on the active and passive components are analysed. Table 2 presents the simulated values for various duty ratios. The Figure 19 and Figure 20 give the comparison between theoretical and simulated output voltages and switch voltages for different duty ratios. The switch voltages and output voltages grow non-linearly as the duty ratio increases. The voltage values rise gradually upto 20% of the duty ratio and increase rapidly beyond that. When the curve is nearer to 25% of duty ratio, the voltages enter into saturation mode. The efficiency and regulation of the suggested converter are represented in Figure 21 and Figure 22 respectively. The proposed converter is designed with a duty ratio of 19% but the highest efficiency point might not occur at this duty ratio.

It is deduced that overall efficiency of the proposed SQZS converter is quite high which is more than 92% even at lower duty ratios. The regulation is under the universal limit of 2% upto the duty ratio of 21%. It can be observed that the losses are very low for the proposed converter. The Figure 23 consists of the capacitor voltage stresses. The capacitor voltages V_{CX} and V_{CY} increase linearly upto 15% of the duty ratio and increases exponentially after that. When the curve is at 23% of duty ratio, the curve enters saturation mode. The output filter capacitor voltage V_{CZ} increases exponentially and enters saturation mode after 23% of the duty ratio. The inductor current stresses represented in Figure 24 rise gradually upto 20% of the duty ratio and increase rapidly beyond that. When the curve is nearer to 24% of duty ratio, the voltages enter saturation mode. The figure 25 represents the input power, output power and power losses of the proposed converter. The difference between the output power and input power is very less. Hence, it can be deduced that the power losses are minimal and the efficiency of the converter is high.

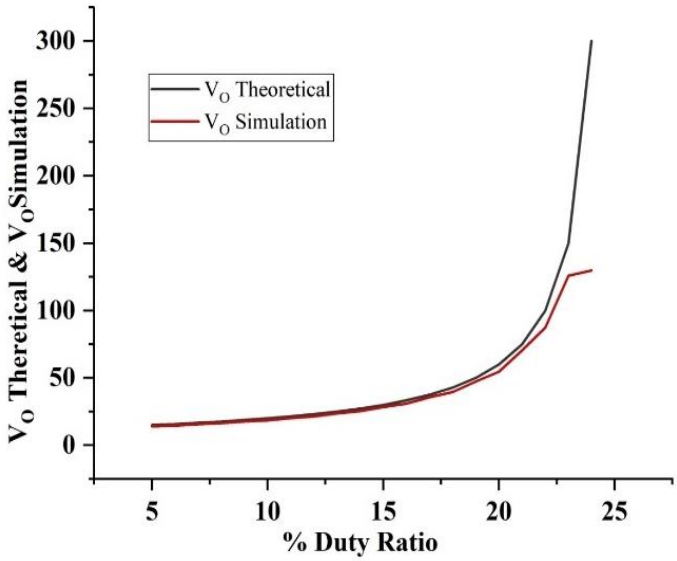


Fig. 19. Comparability between theoretical and simulated output voltages for different duty ratios.

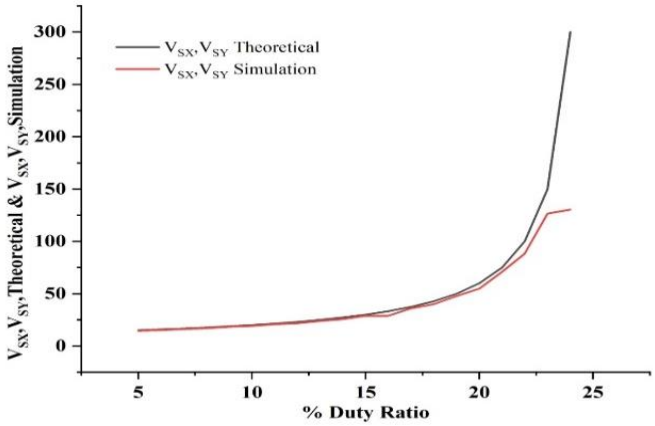


Fig. 20. Comparability between theoretical and simulated output voltages for different duty ratios.

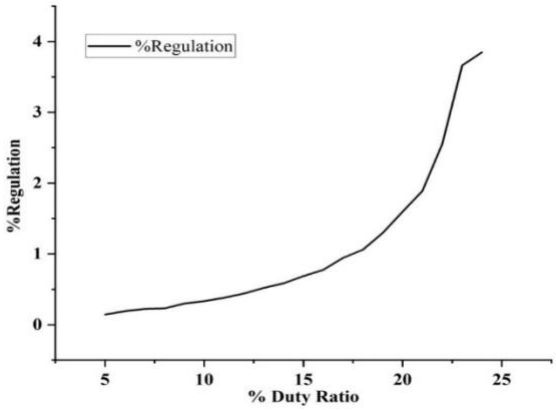


Fig. 21. Relationship between Regulation and duty ratio

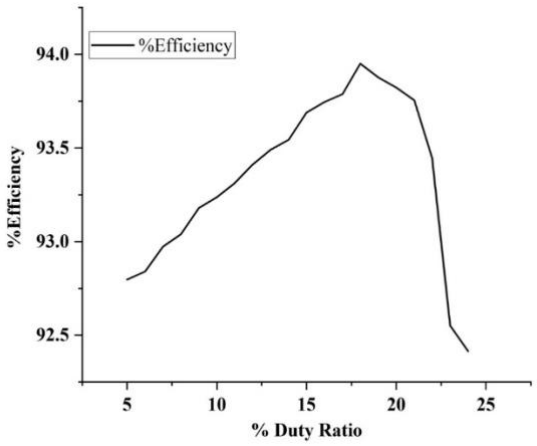


Fig. 22. Relationship between efficiency and duty ratio.

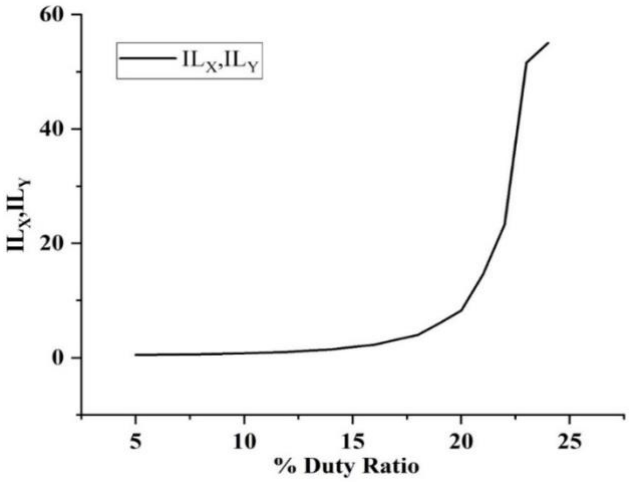


Fig.23. Relationship between capacitor voltage stresses and duty ratio

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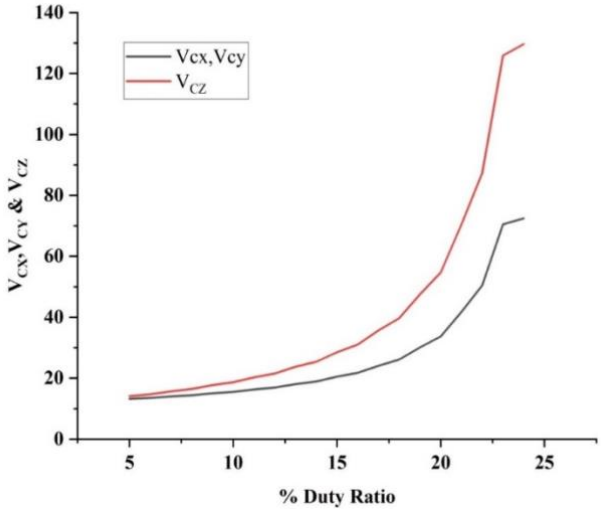

Fig. 24. Relationship between inductor current stresses and duty ratio.

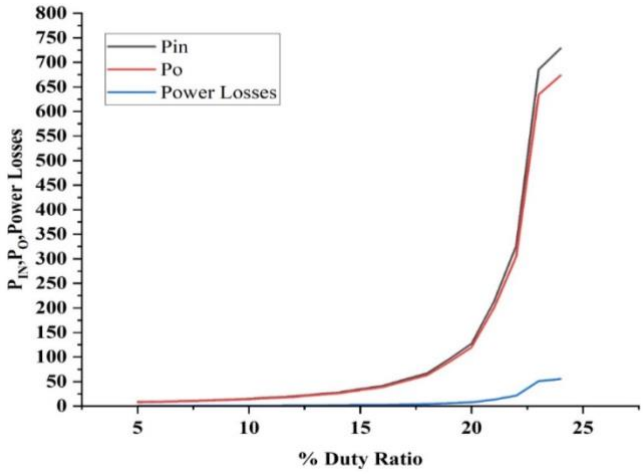

Fig. 25. Relationship between input power, output power, losses and different duty ratios.

6. Conclusions

A Switched Quasi Z-source converter is intended. A higher boost factor of 1/(1-4D) is obtained. When contrasted with the pertinent topologies in provision of energy elements, voltage gain and efficiency, it produces a greater voltage gain with reduced voltage stress and lesser number of energy elements (Inductors and Capacitors) which makes the intended converter cost effective while also being smaller in size and less bulky. The regulation values of the proposed converter are under the universal limit i.e., 2%. The proposed converter can operate at higher efficiencies even for lower duty ratios. A detailed explanation is provided regarding the performing principles, current and voltage parameters of the components. The intended converter is deemed appropriate for photovoltaic applications after the simulation results are collated with the theoretical reasoning.

References

[1]. W. Tushar, J. A. Zhang, C. Yuen, D. B. Smith, and N. Ul Hassan, "Management of renewable energy for a shared facility controller in smart grid," IEEE Access, vol. 4, pp. 4269-4281, 2016.

[2]. A. Shahid, "Smart Grid Integration of Renewable Energy Systems," in 7th International Conference on Renewable Energy Research and Applications, Oct. 14-17, 2018.

[3.] B. S. Goud et al., "Optimization Techniques in PV-Wind based Distribution Generation- A Brief Review," IEEE, pp. 1-6, 2020.

[4]. F. Z. Peng, "Z-source inverter," IEEE Trans. Ind. Appl., vol. 39, no. 2, pp. 504-510, Mar./Apr. 2003.

[5]. L. Yang, D. Qiu, B. Zhang, G. Zhang, and W. Xiao, "A quasi-Z-source DC-DC converter," in Proc. IEEE Energy Convers. Congr. Expo., pp. 941-947, 2014.

[6]. J. Zeng, J. Wu, Z. Yu, and J. Liu, "Switched Z-source DC-DC converter," in Proc. IECON 43rd Annu. Conf., pp. 8039-8044, 2017.

[7]. B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," IEEE Trans. Circuits Syst. I Reg. Papers, vol. 55, no. 2, pp. 687-696, Mar. 2008.

[8]. Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2959-2968, Jun. 2014.

[9]. X. Hu, G. Dai, L. Wang, and C. Gong, "A three-state switching boost converter mixed with magnetic coupling and voltage multiplier techniques for high gain conversion," IEEE Trans. Power Electron., vol. 31, no. 4, pp. 2991-3001, Apr. 2016.

[10]. T. Takiguchi and H. Koizumi, "Quasi-Z-source dc-dc converter with voltage-lift technique," in Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc., pp. 1191-1196, Nov. 10-13, 2013.

[11]. H. Shen, B. Zhang, and D. Qiu, "Hybrid Z-source boost DC-DC converters," IEEE Trans. Ind. Electron., vol. 64, no. 1, pp. 310-319, Jan. 2017.

[12]. S. Rostami, V. Abbasi, and T. Kerekes, "Switched capacitor-based Z-source DC-DC converter," IET Power Electron., vol. 12, no. 13, pp. 3582-3589, Aug. 2019.

[13]. F. Evran and M. T. Aydemir, "Z-source-based isolated high step-up converter," IET Power Electron., vol. 6, no. 1, pp. 117

[14]. Y. Zhang, C. Fu, M. Sumner, and P. Wang, "A wide input-voltage range quasi-Z source boost dc-dc converter with high voltage-gain for fuel cell vehicles," IEEE Trans. Ind. Electron., vol. 65, no. 6, pp. 5201-5212, Jun. 2018.

[15]. D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up DC/DC converters with cascaded quasi-Z-source network," IEEE Trans. Ind. Electron., vol. 59, no. 10, pp. 3727-3736, Oct. 2012.

[16]. M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-Z source DC–DC converter," IEEE Trans. Power Electron., vol. 33, no. 12, pp. 10563-10571, Dec. 2018.

[17]. C. R. Reddy, B. S. Goud, B. N. Reddy, M. Pratyusha, C. V. Vijay Kumar and R. Rekha, "Review of Islanding Detection Parameters in Smart Grids," *2020 8th International Conference on Smart Grid (icSmartGrid)*, Paris, France, 2020, pp. 78-89, doi: 10.1109/icSmartGrid49881.2020.9144923.

[18]. G. S. Rao, B. S. Goud and C. R. Reddy, "Power Quality Improvement using ASO Technique," *2021 9th International Conference on Smart Grid (icSmartGrid)*, Setubal, Portugal, 2021, pp. 238-242, doi: 10.1109/icSmartGrid52357.2021.9551226.

[19]. S. J. Gambhire, M. K. Kumar, K. Mallikarjuna, A. N. Venkateswarlu, C. N. Sai Kalyan and B. S. Goud, "Performance Comparison of Various Classical Controllers in LFC of Hydro-Thermal Power System with Time Delays," *2022 10th International Conference on Smart Grid (icSmartGrid)*, Istanbul, Turkey, 2022, pp. 401-406, doi: 10.1109/icSmartGrid55722.2022.9848690.

[20]. D. Rekioua, T. Rekioua and Y. Soufi, "Control of a grid connected photovoltaic system," *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, Palermo, Italy, 2015, pp. 1382-1387, doi: 10.1109/ICRERA.2015.7418634.

[21]. M. Dahmane, J. Bosche, A. El-Hajjaji and M. Dafarivar, "Renewable energy management algorithm for stand-alone system," *2013 International Conference on Renewable Energy Research and Applications (ICRERA)*, Madrid, Spain, 2013, pp. 621-626, doi: 10.1109/ICRERA.2013.6749830.

[22]. R. Rekha, B. S. Goud, C. R. Reddy, and B. N. Reddy, "PV-Wind-Integrated Hybrid Grid with P&O Optimization Technique," in Innovations in Electrical and Electronics Engineering: Proceedings of the 4th ICIEEE 2019, Springer Singapore, 2020, pp. 587-600.

[23]. H. Gaied, M. Naoui, H. Kraiem, B. S. Goud, A. Flah, M. L. Alghaythi, and K. Aboras, "Comparative analysis of MPPT techniques for enhancing a wind energy conversion system," Frontiers in Energy Research, vol. 10, 2022.

[24]. B. N. Reddy, B. S. Goud, S. Kalyan, C. Naga, P. K. Balachandran, B. Aljafari, and K. Sangeetha, "The Design of 2S2L-Based Buck-Boost Converter with a Wide Conversion Range," International Transactions on Electrical Energy Systems, 2023.

[25]. C. R. Reddy, P. P. Raj, P. V. V. Satyanarayana, B. N. Reddy, O. C. Sekhar, and B. S. Goud, "Improved ZSI-based DVR for Power Quality Improvement in Grid Connected PV Systems," in 2022 4th International Conference on Circuits, Control, Communication and Computing (I4C), IEEE, December 2022, pp. 153-157.

[26]. K. Venkata Govardhan Rao, M. K. Kumar, B. S. Goud, M. Bajaj, M. Abou Houran, and S. Kamel, "Design of a bidirectional DC/DC converter for a hybrid electric drive system with dual-battery storing energy," Frontiers in Energy Research, vol. 10, p. 1732, 2022.

[27] M. Vijayan, R. R. Udumula, T. Mahto, B. Lokeshgupta, B. S. Goud, C. N. S. Kalyan, and B. Twala, "Optimal PI-Controller-Based Hybrid Energy Storage System in DC Microgrid," Sustainability, vol. 14, no. 22, p. 14666, 2022.

[28] V. F. Pires, A. Cordeiro, D. Foito and J. F. Silva, "Control of Bidirectional Quadratic DC-DC Converters for Storage Support of DC Power Grids," *2018 7th International Conference on Renewable Energy Research and Applications (ICRERA)*, Paris, France, 2018, pp. 227-232, doi: 10.1109/ICRERA.2018.8566946.

[29] M. ARAZI, A. PAYMAN, M. B. CAMARA and B. DAKYO, "Control of isolated DC/DC resonant converters for energy sharing between battery and supercapacitors," *2018 7th International Conference on Renewable Energy Research and Applications (ICRERA)*, Paris, France, 2018, pp. 1049-1054, doi: 10.1109/ICRERA.2018.8566965.